IN THE CLAIMS

Claims 1-24   (Canceled)

25.   (New)   A method of manufacturing a semiconductor integrated circuit device, comprising:

forming a plurality of semiconductor chips each having a desired function on a semiconductor wafer;

placing a test circuit connected to conductive needles and configured within programmable logic ICs based on the design data for said each semiconductor chip, which is described in hardware description language and operated in accordance with a program to test said each semiconductor chip, on a probe substrate having a size corresponding to the semiconductor wafer and having the conductive needles formed thereon in alignment with the placement of electrode pads on the semiconductor chips, and provided the programmable logic ICs capable of configuring desired logic in association with the respective semiconductor chips on the semiconductor wafer;

superimposing the probe substrate on the semiconductor wafer in such a manner that the conductive needles are brought into contact with the corresponding electrode pads of the semiconductor chips;

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testing said each semiconductor chip by the test

circuit; and

selecting a semiconductor chip judged to the non-

defective, as a product according to the test.

26.   (New)   The method according to claim 25, wherein

said programmable logic ICs are reconfigured with the design

data for respective associated semiconductor chips which is

described in hardware description language, when the test on a

plurality of semiconductor chips having different functions on

the same semiconductor wafer or the test on a plurality of

semiconductor chips having different respective functions on a

different semiconductor wafer by the probe substrate is

carried out.

27.   (New)   The method according to claim 25, wherein the

test circuit is a test signal generating circuit configured so

as to generate a test signal to each semiconductor chip to be

tested in accordance with a predetermined algorithm.

28.   (New)   The method according to claim 27, wherein the

test signal generating circuit includes:

a memory which holds a program therein;

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a controller which decodes an instruction for the program to thereby generate a control signal; and

a signal generator which generates a signal to be outputted.

29.   (New)   The method according to claim 28, wherein the memory is a rewritable memory.

30.   (New)   The method according to claim 28, wherein the test signal generating circuit further includes:

timing generating means which generates a desired timing signal in response to a reference clock signal as well as timing control data outputted from memory means for holding the timing control data.

31.   (New)   The method according to claim 30, wherein the memory means is a rewritable memory.

32.   (New)   A method of manufacturing a semiconductor integrated circuit device, comprising:

forming a plurality of first semiconductor circuits each having a desired function on a first semiconductor wafer as a first product;

placing a test circuit connected to conductive
needles and operated in accordance with a program to test each
of the plurality of first semiconductor circuits, on a probe
substrate having a size corresponding to the first
semiconductor wafer and having the conductive needles formed
thereon in alignment with the placement of electrode pads on
each of the plurality of first semiconductor circuits, the
test circuit being configured by programmable logic ICs based
on design data for each of the plurality of first
semiconductor circuits;

superimposing the probe substrate on the first
semiconductor wafer in such a manner that the conductive
needles are brought into contact with the corresponding
electrode pads of the plurality of first semiconductor
circuits;

testing the plurality of first semiconductor
circuits by the test circuit; and

selecting a first semiconductor circuit judged to be
non-defective, as the first product according to the test.

33.   (New)   The method according to claim 32, further
comprising:

forming a plurality of second semiconductor circuits each having a desired function different from the desired function of the plurality of first semiconductor circuits on a second semiconductor wafer and each corresponding to a second semiconductor chip as a second product;

reconfiguring the programmable logic ICs with design data for each second semiconductor circuit to reconfigure the test circuit;

superimposing the probe substrate on the second semiconductor wafer in such a manner that the conductive needles are brought into contact with the corresponding electrode pads of the plurality of second semiconductor circuits;

testing the plurality of second semiconductor circuits by the test circuit; and

selecting a second semiconductor circuit judged to be non-defective, as the second product according to the test.

34. (New) The method according to claim 33, wherein the test circuit is a test signal generating circuit configured so as to generate a test signal to each semiconductor chip to be tested in accordance with a predetermined algorithm.

35. (New) The method according to claim 34, wherein the test signal generating circuit includes:

a memory which holds a program therein;

a controller which decodes an instruction for the program to thereby generate a control signal; and

a signal generator which generates a signal to be outputted.

36. (New) The method according to claim 35, wherein the memory is a rewritable memory.

37. (New) The method according to claim 35, wherein the test signal generating circuit further includes timing generating means which generates a desired timing signal in response to a reference clock signal as well as timing control data outputted from memory means for holding the timing control data.

38. (New) The method according to claim 37, wherein the memory means is a rewritable memory.

39. (New) A method of manufacturing a semiconductor integrated circuit device, comprising:

forming a probe substrate which includes a test circuit configured in programmable logic ICs and operated in accordance with a program to test a plurality of first semiconductor circuits to be formed on a first semiconductor wafer, and conductive needles coupled to the test circuit and formed thereon in alignment with a placement of electrode pads on the plurality of first semiconductor circuits, wherein the probe substrate has a size corresponding to the first semiconductor wafer;

forming the plurality of first semiconductor circuits each having a desired function on the first semiconductor wafer and each corresponding to a first semiconductor chip as a first product;

superimposing the probe substrate on the first semiconductor wafer in such a manner that the conductive needles are brought into contact with the corresponding electrode pads of the plurality of first semiconductor circuits;

testing the plurality of first semiconductor circuits by the test circuit; and

selecting a first semiconductor circuit judged to be non-defective, as the first product according to the test.

40.   (New)   The method according to claim 39, further comprising:

when a test on a plurality of second semiconductor circuits having a different function on a second semiconductor wafer by the same probe substrate is carried out, reconfiguring the programmable logic ICs based on design data for each second semiconductor circuit, which is described in hardware description language;

forming the plurality of second semiconductor circuits each having a desired function on a second semiconductor wafer and each corresponding to a second semiconductor chip as a second product;

superimposing the probe substrate on the second semiconductor wafer in such a manner that the conductive needles are brought into contact with the corresponding electrode pads of the plurality of second semiconductor circuits;

testing the plurality of second semiconductor circuits by the test circuit; and

selecting a second semiconductor circuit judged to be non-defective, as the second product according to the test.